

# **APPLICATION FOR UNITED STATES PATENT**

**in the name of**

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**For**

**CLOCK SIGNAL REGENERATION CIRCUITRY**

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# CLOCK SIGNAL REGENERATION CIRCUITRY

## TECHNICAL FIELD

[0001] This invention relates to clock signal regeneration circuitry and more particularly to a common clock signal regeneration circuit adapted for use with either a single ended clock signal source or a differential clock signal source.

## BACKGROUND

[0002] As is known in the art, it is sometimes required to regenerate clock signals at various points in a system. One such system is a data storage system wherein a host computer stores and reads data from a bank of disk drives through a system interface.

[0003] More particularly, large host computers and servers (collectively referred to herein as "host computer/servers") require large capacity data storage systems. These large computer/servers generally includes data processors, which perform many operations on data introduced to the host computer/server through peripherals including the data storage system. The results of these operations are output to peripherals, including the storage system.

[0004] One type of data storage system is a magnetic disk storage system. Here a bank of disk drives and the host computer/server are coupled together through an interface. The interface includes "front end" or host computer/server controllers (or directors) and "back-end" or disk controllers (or directors). The interface operates the controllers (or directors) in such a way that they are transparent to the host computer/server. That is, data is stored in, and retrieved from, the bank of disk drives in such a way that the host computer/server merely thinks it is operating with its own local disk drive. One such system is described in U.S. Patent 5,206,939, entitled "System and Method for Disk Mapping and Data Retrieval", inventors Moshe Yanai, Natan Vishlitzky, Bruno Alterescu and Daniel Castel, issued April 27, 1993, and assigned to the same assignee as the present invention.

[0005] As described in such U.S. Patent, the interface may also include, in addition to the host computer/server controllers (or directors) and disk controllers (or directors), addressable cache memories. The cache memory is a semiconductor memory and is provided to rapidly store data from the host computer/server before storage in the disk drives, and, on the other hand, store data from the disk drives prior to being sent to the host computer/server. The cache

memory being a semiconductor memory, as distinguished from a magnetic memory as in the case of the disk drives, is much faster than the disk drives in reading and writing data.

[0006] The host computer/server controllers, disk controllers and cache memory are interconnected through a backplane printed circuit board. More particularly, as described in U. S. Patent No. 6,289,401, issued September 11, 2001 and assigned to the same assignee as the present invention, the entire subject matter thereof being incorporated herein by reference, disk controllers are mounted on disk controller printed circuit boards and data therein passes to the backplane and then to the disk drive through an adapter board. Likewise, the host computer/server controllers are mounted on host computer/server controller printed circuit boards and data therein passes to the backplane and then to the host computer/server through an adapter board.

[0007] As is also known in the art, each one of the directors includes a clock for producing clock signals associated with data being processed by such director. In some applications, it may be desirable to regenerate these clock signals for data passing through the adapter boards. However, some director boards may operate with GigE type signals and therefore use a clock which produces single-ended clock pulses such as are generated with TTL (transistor-transistor logic) logic circuitry. In some applications it may be desirable to have the directors operate with fibre channel, Ficon or Escon type signals. Therefore, it is necessary to replace the TTL single-ended clock used on directors with a differential clock, such as are generated with PECL (i.e., positive emitter coupled logic) logic circuitry. However, it would be desirable if the adapted board clock regeneration circuitry not require changing to accommodate this change in director board clock circuitry.

## SUMMARY

[0008] In accordance with the present invention a method is provided for regenerating clock signals. The method includes converting clock signals having either single-ended clock pulses or differential clock pulses into clock signals having substantially the same voltage swing.

[0009] In one embodiment, the single-ended clock pulses are provided by a TTL logic circuit and the differential clock pulses are produced by an ECL logic circuit. In one embodiment, the ECL logic circuit is a PECL logic circuit.

[0010] In accordance with another feature of the invention, a method is provided for regenerating clock signals. The method includes providing a source of clock signals, such source producing either single- ended clock pulses or differential clock pulses. The clock signals are fed to a regeneration circuit. The regeneration circuit converts such clock signals having either the single- ended clock pulses or the differential clock pulses into clock signals having substantially the same voltage swing.

[0011] In accordance with another feature of the invention, a clock regeneration circuit is provided. The circuit includes: a differential amplifier having a non-inverting input terminal and an inverting input terminal; a first voltage divider network coupled between a pair of reference voltages and the non-inverting input terminal; a second voltage divider network coupled between the pair of reference voltages and the inverting input terminal. The first and second voltage divider networks produce the same voltage at the inverting and non-inverting input terminals.

[0012] In one embodiment, the first voltage divider network includes a pair of resistors, a first one of the pair of resistors, R1, being connected between a first one of the pair of reference voltages and the non-inverting input and a second one of the pair of resistors, R2, being connected between the non-inverting input and the second one of the pair of reference voltages.

[0013] In one embodiment, the second voltage divider network includes a pair of resistors, a first one of the pair of resistors, R3, being connected between a first one of the pair of reference voltages and the inverting input and a second one of the pair of resistors, R4, being connected between the inverting input and the second one of the pair of reference voltages.

[0014] In one embodiment, R1 is has the same resistance as R3 and R2 has the same resistance as resistor R4.

[0015] In one embodiment, a transmission line is coupled between a source of clock signals and the input terminals. The transmission line has a characteristic impedance  $Z_o$ , and  $R1 \cdot R2 / (R1 + R2)$  equals  $Z_o$ .

[0016] In one embodiment, the source of clock pulses is an emitter coupled logic circuit and wherein the potential difference provided by the pair of reference voltages voltage,  $V_{cc}$ , times  $(R2 / (R1 + R2))$  and  $V_{cc}$ , times  $(R3 / (R3 + R4))$  are selected to provide predetermined proper terminating voltages to the emitter coupled logic circuit.

[0017] In one embodiment, the source of clock pulses is a transistor-transistor logic circuit having an output transistor, such output transistor having an emitter and collector coupled between the pair of reference potentials. A coupling resistor R5 is serially connected between the collector electrode and the non-inverting input through the transmission line,  
5 such resistor R5 being selected to provide a predetermined proper voltage swing across the non-inverting and inverting inputs

[0018] The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

## DESCRIPTION OF DRAWINGS

[0019] FIG. 1 is a block diagram of a source of clock pulse coupled to a clock pulse regeneration circuit according to the invention;

[0020] FIG. 2 is a block diagram of a source of single-ended clock pulses to the clock pulse regeneration circuit according to the invention;

15 [0021] FIG. 3 is a schematic diagram of an output portion of a TTL logic circuit used in the source of single-ended clock pulse of FIG. 2;

[0022] FIG. 4A is an equivalent circuit of the source of single-ended clock pulse of FIG. 2 when a transistor used in the output portion is conducting;

[0023] FIG. 4B is an equivalent circuit of the source of single-ended clock pulse of  
20 FIG. 2 when a transistor used in the output portion is non-conducting;

[0024] FIG. 5 are curves showing voltages produced by the TTL logic circuit of FIG. 3;

[0025] FIG. 6 is a curve showing the clock pulses produced by the a clock pulse regeneration circuit of FIG. 2;

25 [0026] FIG. 7 is a block diagram of a source of differential clock pulses coupled to the clock pulse regeneration circuit according to the invention;

[0027] FIG. 8 are curves showing voltages produced by the source of differential clock pulses of FIG. 7; and

[0028] FIG. 9 is a curve showing the clock pulses produced by the a clock pulse  
30 regeneration circuit of FIG. 8..

[0029] Like reference symbols in the various drawings indicate like elements.

## DETAILED DESCRIPTION

[0030] Referring now to FIG. 1 a director board 10 is shown coupled to an adapter board 12 through a backplane 14. The director board 10 includes a clock signal source 16 for producing clock pulses, such clock pulses being transmitted to the adapter 12 through a transmission line 20. The adapter board 12 includes a clock regeneration circuit section 22. The clock signal source may include either a TTL logic circuit transmitter (i.e., for producing the single-ended clock pulses) or an ECL logic circuit transmitter, here a PECL logic circuit transmitter (i.e., for producing differential clock pulses). In either case, the clock regeneration circuit section 22 converts the clock signals produced by the clock signal source 16 (having either the single-ended clock pulses or the differential clock pulses) to clock signals having substantially the same voltage swing.

[0031] Referring to FIG. 2, the clock signal source 16 in FIG. 1, includes an oscillator 24 coupled to a TTL logic circuit transmitter 26' (i.e., for producing the single-ended clock pulses) to provide a TTL clock signal source 16', as shown. The output section of the TTL logic circuit transmitter 26' is shown in more detail in FIG. 2 to include a grounded emitter transistor having a collector coupled to Vcc, here 3.3 volts through a pull up resistor RL. Thus, the output of the transmitter 26' produces a single ended train of clock pulses on line 20' of the transmission line 20.

[0032] Referring again to FIGS. 1 and 2, the adapted board 12, as noted above, includes a clock regeneration circuit section 22. The section 22 includes a differential amplifier 30 (or receiver) having a non-inverting input terminal (+) and an inverting input terminal (-). A first voltage divider network 32 is coupled between a pair of reference voltages, here +Vcc and ground, and the non-inverting input terminal (+). A second voltage divider network 34 is coupled between the pair of reference voltages, (i.e., +Vcc and ground) and the inverting input terminal (-). The first and second voltage divider networks 32, 34 produce the same voltage at the inverting (-) and non-inverting input terminals (+).

[0033] More particularly, the first voltage divider network 32 includes a pair of resistors, R1, R2. A first one of the pair of resistors, R1, is connected between a first one of the pair of reference voltages, here +Vcc, and the non-inverting input (+) and a second one of the pair of resistors, R2, is connected between the non-inverting input (+) and the second one of the pair of reference voltages, here ground.

[0034] The second voltage divider network 34 includes a pair of resistors, R3, R4. A first one of the pair of resistors, R3, is connected between a first one of the pair of reference voltages, here +Vcc, and the inverting input (-) and a second one of the pair of resistors, R4, is connected between the inverting input (-) and the second one of the pair of reference voltages, here ground.

[0035] The resistor R1 has the same resistance as R3 and R2 has the same resistance as resistor R4. Here, in this example,  $R1=R3=124$  ohms and  $R2=R4=82.5$  ohms

[0036] It is noted that the transmission line 20 is used to couple the source of clock signals 16 (FIG. 1) and the input terminals (+), (-). The transmission line 20 has a characteristic impedance  $Z_o$ , here 50 ohms. It is noted that the transmission line 20 is terminated in this characteristic impedance,  $Z_o$ . Thus,  $R1 \cdot R2 / (R1 + R2) = R3 \cdot R4 / (R3 + R4) = Z_o$ .

[0037] Referring now to FIGS. 4A and 4B, FIG. 4A shows an equivalent circuit for the transistor in the output section of the TTL logic circuit transmitter 26', shown in FIG. 3, when such transistor is conducting, here represented by a resistor  $R_{e\_lo}$  here 20 ohms, and FIG. 4B shows an equivalent circuit for the transistor, with pull-up resistor  $R_L$ , when such transistor is non-conducting, here represented by a resistor  $R_{e\_ho}$  here 33.5 ohms. It is also noted in FIGS. 2 and 3 that the clock signal source 16' includes a coupling resistor R5 serially connected between the collector electrode and the non-inverting input (+) through the line 20<sub>1</sub> of transmission line 20. The resistor R5 is included in the equivalent circuits shown in FIGS. 4A and 4B. As noted above, line 20<sub>1</sub> is connected to the non-inverting input (+) and to the first voltage divider network 32.

[0038] Referring to FIG. 2, line 20<sub>2</sub> of the transmission line is connected to ground through a dc blocking capacitor, here 5pf, and serially connected resistor R6, here 50 ohms. The resistor R6 is selected to match the characteristic impedance of the transmission line 20, Thus, as also noted above, and referring to FIG. 2, the inverting input terminal (-) is connected to the second voltage divider network 34. The resistor R5 is selected to provide a predetermined proper voltage swing across the non-inverting and inverting inputs. Thus, here resistor R5 is 60 ohms. Thus, when the transistor is conducting, FIG. 4A, the voltage on line 20<sub>1</sub> is 0.8 volts and when non-conducting, FIG. 4B, the voltage on line 20<sub>1</sub> is here 2.0 volts. The second resistor divider network 34, FIG. 2 produces a voltage of 1.3 volts on line 20<sub>2</sub>. Thus, as shown in FIG. 5, the voltage on line 20<sub>1</sub> (i.e., at the non-inverting input (+))

swings between about 2.0 volts and 0.8 volts while the voltage on line 20<sub>2</sub> remains substantially at 1.3 volts. In response to the voltages shown in FIG. 5, the clock pulse regeneration circuit section 32, FIG. 2, produces clock pulses shown in FIG. 6, such clock pulses having a voltage swing between about +0.7 volts and -0.5 volts.

5           [0039] Referring now to FIG. 7, the TTL logic circuit transmitter 26' (i.e., for producing the single- ended clock pulses) is replaced with an ECL logic circuit transmitter 26", here a PECL logic circuit. The potential difference provided by the pair of reference voltages voltage, V<sub>cc</sub>, times (R<sub>2</sub>/(R<sub>1</sub>+R<sub>2</sub>)) and V<sub>cc</sub>, times (R<sub>3</sub>/R<sub>3</sub>+R<sub>4</sub>) are selected to provide predetermined proper terminating voltages to the emitter coupled logic circuit. Thus, here  
10       the resistors R<sub>1</sub> and R<sub>2</sub> are selected to provide +1.3 volt on line 20<sub>1</sub> (i.e., at the non-inverting input (+)) and the resistors R<sub>3</sub> and R<sub>4</sub> are selected to provide +1.3 volt on line 20<sub>2</sub> (i.e., at the inverting input (-)). As noted above, in order to match load terminate the transmission line 20,  $R_1 \cdot R_2 / (R_1 + R_2) = R_3 \cdot R_4 / (R_3 + R_4) = Z_0 = 50$ . Therefore, to satisfy these relationships, R<sub>1</sub>=R<sub>3</sub>=124 ohms and R<sub>2</sub>=R<sub>4</sub>= 82.5 ohm. It is noted that these values for R<sub>1</sub>, R<sub>3</sub>, R<sub>2</sub> and  
15       R<sub>4</sub> were used in connection with the TTL transmitter 16' described above in connection with FIGS. 2, 3, 4A and 4B. Thus, the same clock regeneration circuit section 22 is used for either the TTL logic circuit transmitter 26' (i.e., for producing the single- ended clock pulses) is replaced with an ECL logic circuit transmitter 26" (i.e., for producing differential clock pulses).

20           [0040] Referring now to FIG. 8, the voltage swing on line 20<sub>1</sub> (i.e., at the non-inverting input (+)) relative to ground is shown in the curve labeled 50 in FIG. 8. It is noted that the voltage swing is between about +2.2 volts and +1.5 volts. The voltage swing on line 20<sub>2</sub> (i.e., at the inverting input (-)) relative to ground is shown in the curve labeled 52 in FIG. 8. It is noted that the voltage swing is also between about +2.2 volts and +1.5 volts.

25           [0041] In response to the voltages shown in FIG. 8, the clock pulse regeneration circuit section 32, FIGS. 2 and 7, produces clock pulses shown in FIG. 9, such clock pulses having a voltage swing between about +0.7 volts and -0.7 volts. Thus, the voltage swing is substantially the same as the voltage swing shown in FIG. 6. Thus, the clock pulse regeneration circuit section 32, FIGS. 2 and 7, converts clock signals having either the single-  
30       ended clock pulses (i.e., from TTL logic circuit transmitter 26') or the differential clock pulses to clock signals (i.e., from ECL logic circuit transmitter 26") to clock pulses having substantially the same voltage swing.



[0042] A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Accordingly, other embodiments are within the scope of the following claims.